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		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L3	L2 and ((buffer or array) near2 (trace or traced or tracing))	132
☐	L2	debug$ near2 (circuit or chip or module)	2478
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L12: Entry 5 of 7 File: USPT Sep 2, 2003

US-PAT-NO: 6615370
DOCUMENT-IDENTIFIER: US 6615370 B1

TITLE: Circuit for storing trace information

DATE-ISSUED: September 2, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Edwards; David Alan	Bristol			GB
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US-CL-CURRENT: 714/45

ABSTRACT:

A system for performing non-intrusive trace is provided which receives trace information from one or more processors. The trace system may be configured by a user to operate in various modes for flexibly storing or transmitting the trace information. The trace system includes a FIFO which is memory-mapped and is capable of being accessed without affecting processor performance. In one aspect, the trace system includes a trace buffer which receives trace information at an internal clock speed of the processor. In another embodiment, a compression protocol is provided for compressing trace messages on-chip prior to transmitting the messages to an external system or storing the messages in memory.

26 Claims, 12 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 11

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